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Power Analysis of Quantum Cellular Automata Circuits

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Abstract

Quantum cellular automata technology (QCA) is one of the promising nanotechnologies in future due to the prospects of extremely low power operation and reduction of interconnections. This paper discuss about energy flow equations, calculation of power dissipation for elementary QCA circuits. The upper bound power model of QCA Cell from its energy flow equations can be used to calculate power gain and power dissipation of QCA Circuits. This upper bound model can be used to find error due to the information flow in a QCA circuit. Hence power dissipation of majority gate, invertors, multiplexer and OR – serial array of QCA circuits are studied and estimated. It was found that higher power dissipation for unlikely inputs than the same type of inputs. The calculated theoretical power gain of QCA cell in or –serial array QCA circuit gives the same results and the simulation results are validated. The proposed QCA Power analysis method can be used to find the power dissipation of a complete QCA system and also to detect polarization error in any type of QCA circuits.

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Keywords:Quantum cellular Automata, Quantum dots, Hamiltonian Equations, Power dissipation and Majority Gate.

1. Main text

The conventional transistor based CMOS technology has followed Moore's law. The size of the transistor reduction has been the major trend to achieve circuits with fast speed, high density and low power dissipation. QCA as emerging technology beyond current transistor switches to encode binary information. Quantum dots are nanostructures created from standard semi conductive materials. These structures are modelled as quantum wells. A.Vetteh et al,(2002).They exhibit energy effects even at distances several hundred times larger than the material system lattice constant. A dot can be visualized as well. Once electrons are trapped inside the dot, it requires higher energy for electron to escape. Quantum dot cellular automata is a Novel technology that attempts to create general computational functionality at the nanoscale by controlling the position of single electrons K.walus et al(2004). The fundamental unit of QCA is QCA cell created with four quantum dots positioned at the vertices of a square K walus

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Dimitriv et al (2003). The electrons are quantum mechanical particles; so they are able to tunnel between the dots in a cell. The electrons in the cell that are placed adjacent to each other will interact; as a result the polarization of one cell will be directly affected by the polarization of its neighbouring cells. Fig 1 shows quantum cells with electrons occupying opposite vertices. K.walus et al(2004)

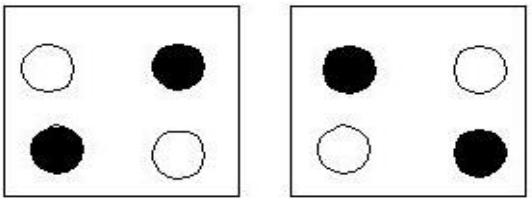

Fig 1 QCA cells with four quantum dots.1 (a) P = +1 (Binary 1) 1(b) P = -1 (Binary0) K.walus and Jullian etal (2004)

This interaction forces between the neighbouring cells able to synchronize their polarization. Therefore an array of QCA cells acts as wire and is able to transmit information from one end to another K.Walus and schulf (2004). Thus the information is coded in terms of polarization of cell. Polarization of each cell depends on polarization of its neighbouring cells. Both theoretically and experimentally a significant amount of research has been done in QCA and ensures primary candidate for nano computing. It encodes the binary information in terms of charge configuration within the cell. The columbic interaction between the cells accomplish computing in QCA arrays, therefore no interconnect and noncurrent flow out of cell, hence low power dissipation is possible K.walus and wang et al (2004). Following this introduction, next section reviewed the energy flow equation in a QCA circuit to calculate polarization, energy and power dissipation of a QCA cell, then discussed about calculation of power dissipation of QCA circuits, the upper bound power model of a QCA circuit is calculated from the proposed method and finally the theoretical power gain calculation of any type of QCA array circuit is described in detail.

2. Energy and Power dissipation Calculation of QCA cell

The worst case Power estimate of a QCA cell can be found by considering non- adiabatic clocking scheme, the upper limit of power dissipation of quantum cellular automata circuits are calculated. Each QCA cell is denoted by Eigen states as |1> and |0>. Quantum mechanical calculations are required to find the power dissipation and polarization of a QCA cell. The Schrödinger wave equation for the wave function at a given time t is Hamiltonian, Equation 1 and 2 is Hamiltonian equation in matrix format.

$$\mathrm{Hj} = \begin{bmatrix} \dfrac{-Ek}{2\Sigma Fj,mPm} & -\gamma \\ -\gamma & \dfrac{Ek}{2\Sigma Fj,mPm} \end{bmatrix} \tag{1}$$

$$\mathrm{Hj} = \begin{bmatrix} \dfrac{-EkP}{2} & -\gamma \\ -\gamma & \dfrac{EkP}{2} \end{bmatrix} \tag{2}$$

Hamiltonian equation is 2 X 2 matrix solved from Schrödinger wave equation through hard tree fock

approximation method. Let γ be the tunnelling energy between two polarized states (p =1 and p = -1) and P = 0 be the null state, E_c be the potential energy, E_k be the kink energy. The kink energy is defined as the energy difference between two horizontally adjacent polarized cells having same or opposite polarizations. $F_{j,\,m}$ is geometric factor which depends on distance and orientation of j^{th} QCA cell and its neighbouring m^{th} QCA cell.($f_{j,m} = 1$). Pm be the polarization of the cell considered.QCA has four dots with electrons confined in two dots of the cell, state vector representation is needed to find the polarization state of the electrons in a QCA cell. The quantum mechanical description of state vector is **λ'** coherence vector which is straight forward to find polarization and dissipation effects of QCA cell. The expected value of any observable, **A'(t)** can be expressed in terms of the wave function as **<A'(t)> = <Ψ(t)|A'(t)|Ψ(t)>** or equivalently as **Tr[A'(t)|Ψ(t)Ψ'(t)|],** where **Tr** denotes the trace operation, **Tr[⋯] = _1|⋯|1_+_0|⋯|0_**. The term **|Ψ(t)><Ψ(t)|** is known as the density operator, **ρ(t).** Expected value of any observable of a quantum system can be computed if **ρ(t)** is known. The energy flow H'can be found from the density matrix and Hamiltonian equations. When the clock level is at high or barriers are raised then there will be energy flow into the cell and when the clock is at low level or barriers are lowered and energy is returned to the clock.

The net flow of energy in the circuit is given by equation 3.

$$E_{net} = Ein + Eclock + Eout + Ediss \tag{3}$$

In steady state net energy must be zero, the sign of the input energy must be positive and sign of output energy and energy dissipated are negative. Power flow in the cell can be written as by differentiating energy equation as given J.timler and C.s.Lent (2002). From equations 1 to 3, it can be found that the upper limit for the energy dissipated by a QCA cell during the switching event.

$$Ediss = [2\gamma new / Ek\ (\frac{Po}{Pold}\gamma old - \frac{Pn}{P'new}\gamma new) + Ek\ \frac{P'new}{2}(Pn - Po)] \tag{4}$$

If τ be the energy relaxation time then the power dissipated can be found

$$Pdiss = 1/\tau[2\gamma new / Ek\ (\frac{Po}{Pold}\gamma old - \frac{Pn}{P'new}\gamma new) + Ek\ \frac{P'new}{2}(Pn - Po)] \tag{5}$$

Let Pn and Po be the polarization of the input and output cell, P_{old} and P'_{new} be the polarization before and after switching of the QCA cell, γ_{new} and γ_{old} are the clock energy during switching event. Equations 4 and 5 are the net energy and power dissipation of a basic qca cell

2. Power dissipation in QCA Circuits.

QCA cells are grouped in a column structure for energy study. The power dissipation of QCA circuits with the clock value between 0.3 to 0.7 Ek (Maximum kink energy between two QCA cells) are applied to the basic QCA circuit and total power dissipation can be found as in J.Timler and CS Lent (2002). Figure2(a) and (b), 3 and 4 shows the column layout diagram of majority gate, nand gate, multiplexer and serial OR array. It is verified that the total energy calculated by these simulations is same as that of quantum simulations by J.timler and C.S.Lent (2002). Figure 5 (a) and (b) shows the power dissipation of majority logic gates when input switched from 111 to 111 and from 110 to 111. Also it is observed for switching 111, the total power dissipation is due to raising and lowering the clock only. But for a switching event of 110 to 111, the polarization changes and hence more power dissipation than 111 switching event. The highest power dissipation in the Majority gate circuit is the output cell of 63 Mlli eV when switching from 111 to 111. Majority gate output cell has higher power dissipation than the other cell due to the availability of output for lowering the clock. For a switching event, output cell has to replicate the majority of inputs, so when one of the inputs differ and the power dissipation of center QCA cell includes not only clock but also change in the polarization, 1 to 0 or 0 to 1.

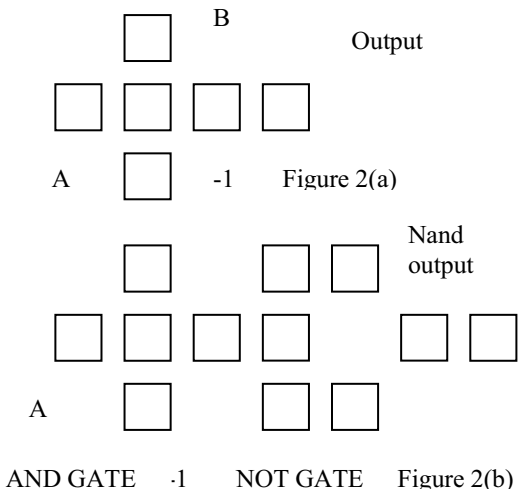

Figure 2 (a) and (b) Layout (column) representation of Majority gate and Nand gate

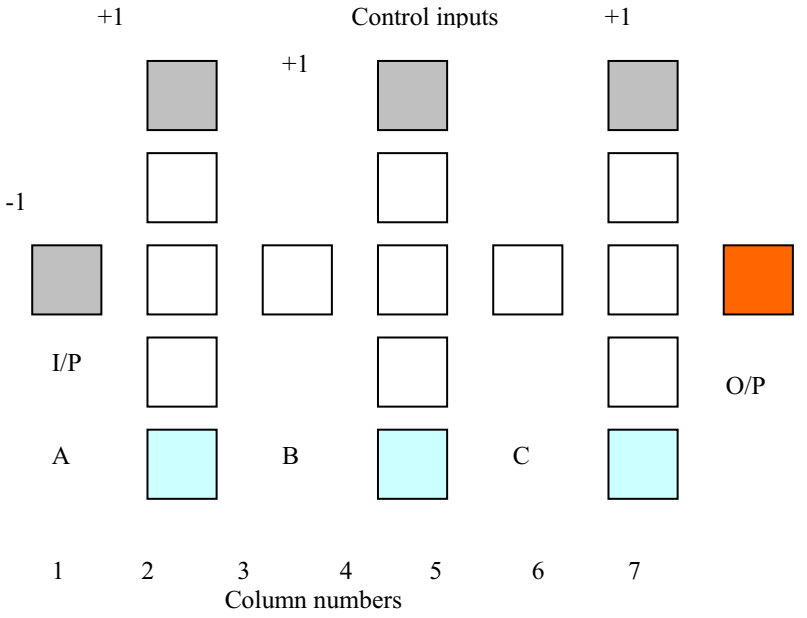

Figure 3 Layout (column) representation of Serial OR array QCA circuit.

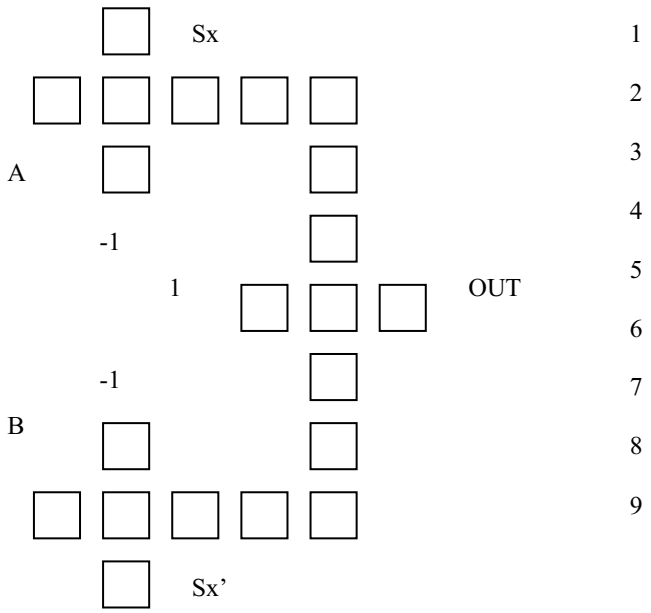

Figure 4 Layout (column) representation of 2:1 Multiplexer

Figure 5 (a) and (b) shows the polarization change at the centre of the cell when one of the input differs , so power dissipation is higher for an switching event of 110 to 111 and power dissipation of center cell in QCAarray is 71 Milli eV. Figure 6 and 7 shows the power dissipation calculated for individual QCA cells in Nand gate and 2:1 Multiplexer. It is considered for QCA Nand gate the switching behavior of 110 to 111 which has AND and Inverter circuit, inputs to the AND gate are 1, 1, 0 and the power dissipation for the center cell is higher than the output cell, but the inverter connected to the AND gate has higher power dissipation than majority AND gate. From figure 6 columns 6 and 7 has more power dissipation than nearby columns due to inversion of 1 to 0. The highest power dissipation in the inverter circuit is 118 Milli eV at column 6. Multiplexer has higher power dissipation at column no 5 and 6 of centre QCA cell as shown in figure 7. Figure 8 shows the QCA or array and power dissipation of switching 110 to 111. It is observed that the column no 2 of center QCA cell in the first majority gate has power dissipation of 63 Miili eV due to switching of 110 to 111, other QCA cells shows lesser power dissipation due to switching of 111 to 111. In conclusion that upper bound power model dissipation may vary depending on switching of inputs which could be traced easily in a QCA system by this analysis.

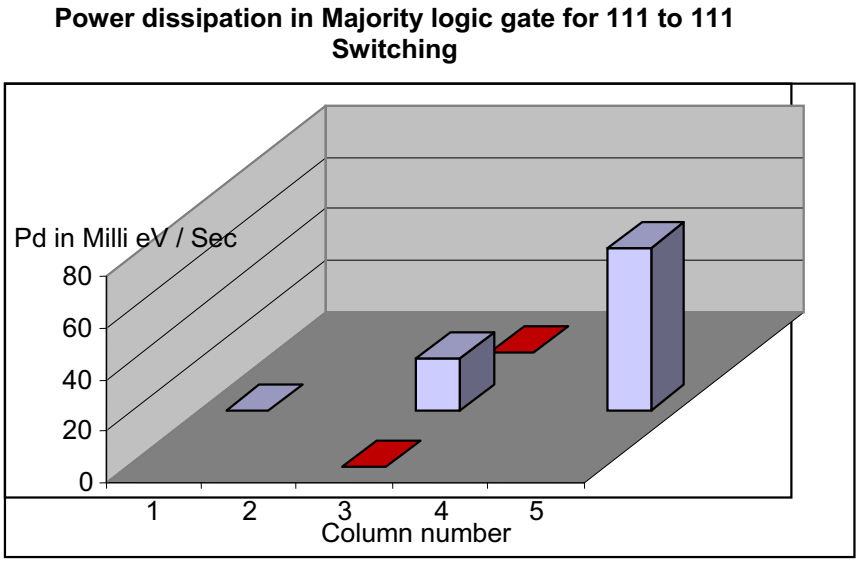

Figure 5 (a) Power dissipation in Majority logic during switching of 111 to 111.

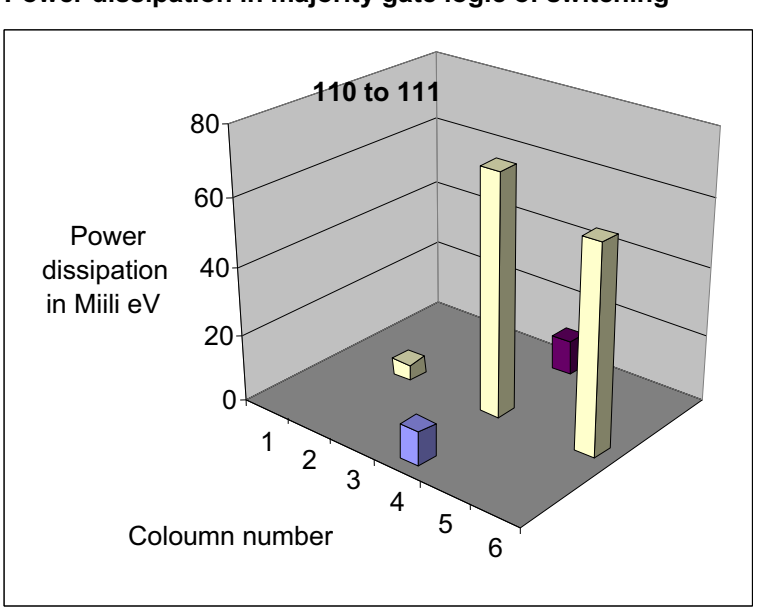

Figure 5 (b) Power dissipation in Majority gate during switching 110 to 111.

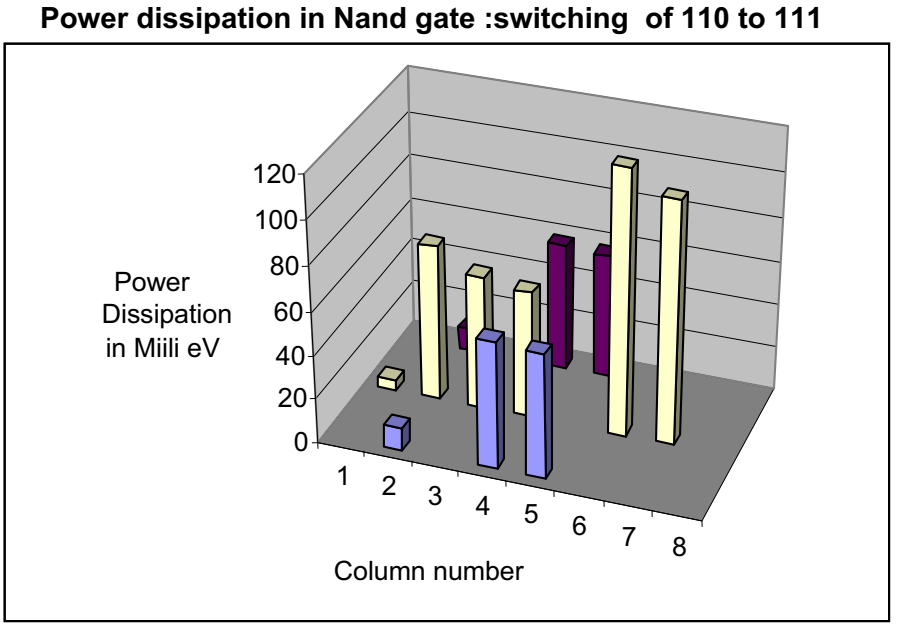

Figure 6 Power dissipation in Nand gate during switching 110 to 111.

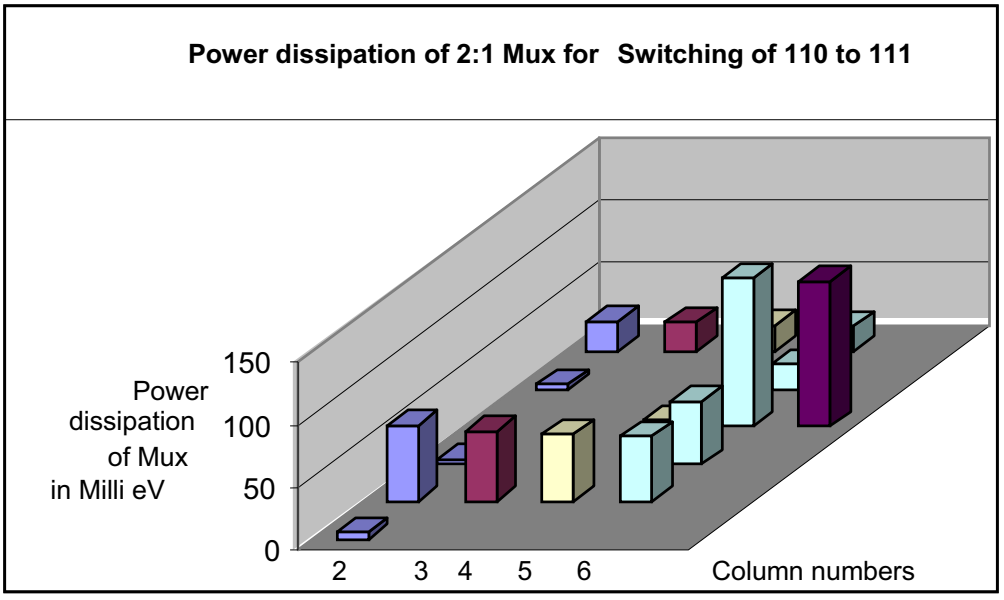

Figure 7 Power dissipation in 2:1 Multiplexer during switching of 110 to 111

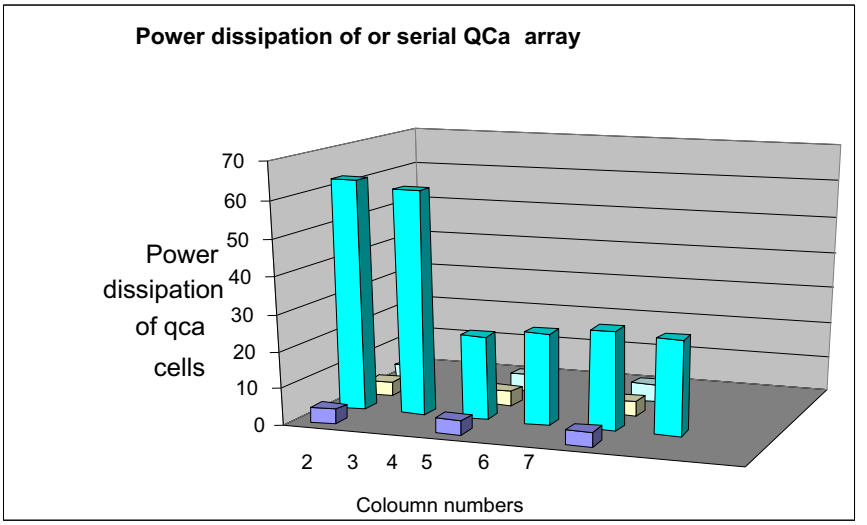

Figure 8 Power dissipation of QCA cells in Serial QCA OR Array, 111 to 110 switching.

3. Theoretical Power gain calculations in QCA circuits

QCA Majority array circuit in OR Serial is taken as example to explain theoretical explanation of power gain. QCA or-Array circuit has three Majority gate structure. A sequence of phase shifted clock is applied through the array, initially all clocks are off and all gates are in null state. The initial energy flow in a majority gate is such that each majority gate (three majority gates are considered for energy transfer) transfers the energy in serial manner in QCA array circuit. The work done on the majority gate by nearby gates or vice versa constitutes energy flow. The clock applied to majority gate acts as external signal and used as energy source or sink of the majority gate. It is easy to measure energy over the input and output of the gate over one clock cycle. Figure 9 a shows the majority And gate and 9(b) shows the equivalent cell representation using QCADesigner tool. The work done on the qca cell in a majority gate over one clock cycle is given by equation 26.

$$w = \int VdQ = \int_0^t V(t)dQ(t)/dt.dt \tag{6}$$

Where $V_L(t)$ is voltage applied to the lead of majority gate, Q(t) be the charge on the capacitor coupling due to voltage applied.

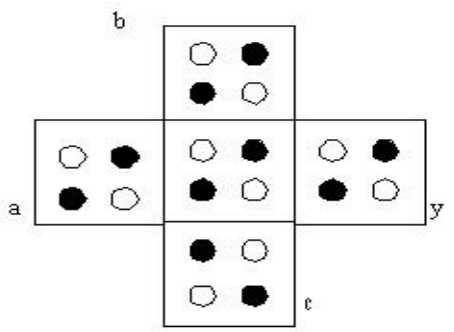

Figure 9 (a) Majority And gate (a = 1, b=1,Control input = 0, y = 1) K.Walus etal (2004)

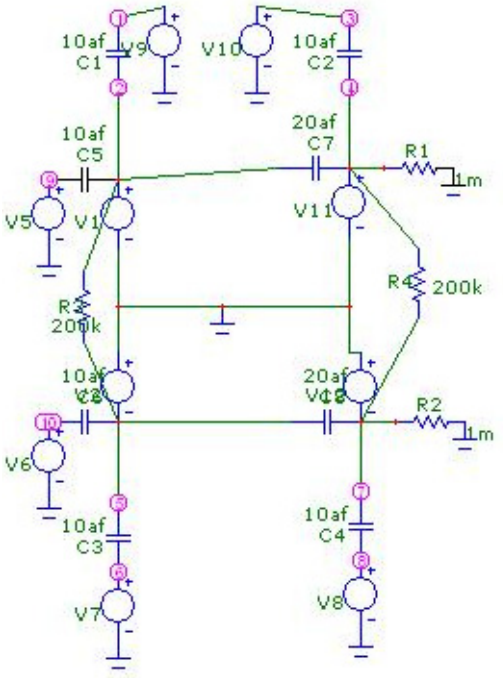

Figure 9 (b) Equivalent cell representation of Single Majority gate of QCA cell, Spectrum – soft (Microcap)
V1= V2 = V11 = V12 = 10 mv, R1 = R2 = R3 = R4 = 200K as in Tang and Zand (2005).

Each cell has voltage source and a capacitor, middle cell has a dot can be visualized as RC circuit (R- tunnel resistance and C-capacitance) with voltage source of 10 microvolt. Let Vin be the voltage applied through the capacitor C5 and the charge in the capacitor is given as

$$Q(t) = C5\,[\,V5(t) - V1(t)]. \tag{7}$$

Now the power gain is defined as ratio of output power to input power

$$PowerGain = \frac{Pout}{Pin} = \frac{\frac{Wout}{T}}{\frac{Win}{T}} \tag{8}$$

If the input to the gate is relatively 10 milli volts it is enough for the direction of switching, then clock here is to be applied for the circuit to provide additional energy for required switching, as shown in figure 9(b) V7, V8, V9 and V10 used to give additional voltage through the capacitors C1, C2 ,C3 and C4. Three QCA cells with their dots occupying electrons considered equivalent to a voltage source and capacitor. The resistance with the capacitor and voltage source acts as equivalent dot or reservoir to store an electron. To demonstrate power gain for the circuit, single majority gate with a weak signal as input, a signal of 100 micro volts applied to the center cell through capacitor of 10 af and center cell has capacitor of 20 af with the voltage of 100 micro volts. A pulse signal of 100micro volts is applied to the center cell and the above circuit is simulated. Figure 10 shows the pulse signal applied to the QCA cell. Figure 11 shows the simulated output voltage across R1 and R2. The majority logic of available inputs are reflected at the center of a QCA cell, So both the signal and its inversion are available at the center of a QCA cell.

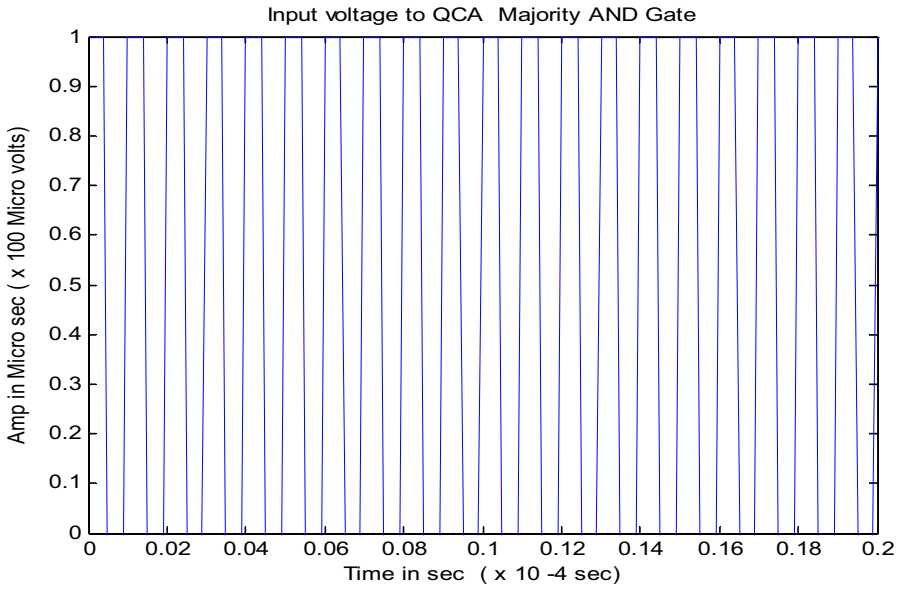

Figure 10 Input voltage to QCA circuit in Majority And gate

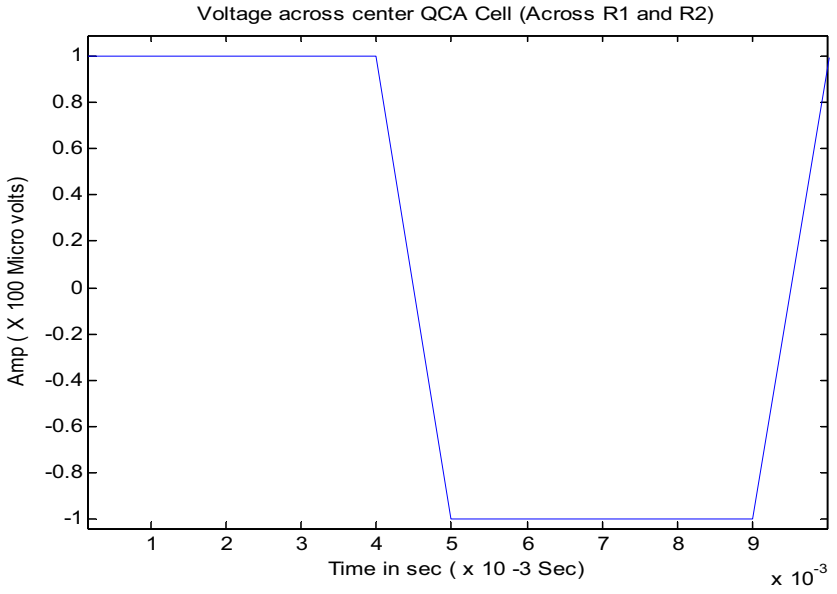

Figure 11 Voltage across Control center QCA cell (across the resistance R1 and R2).

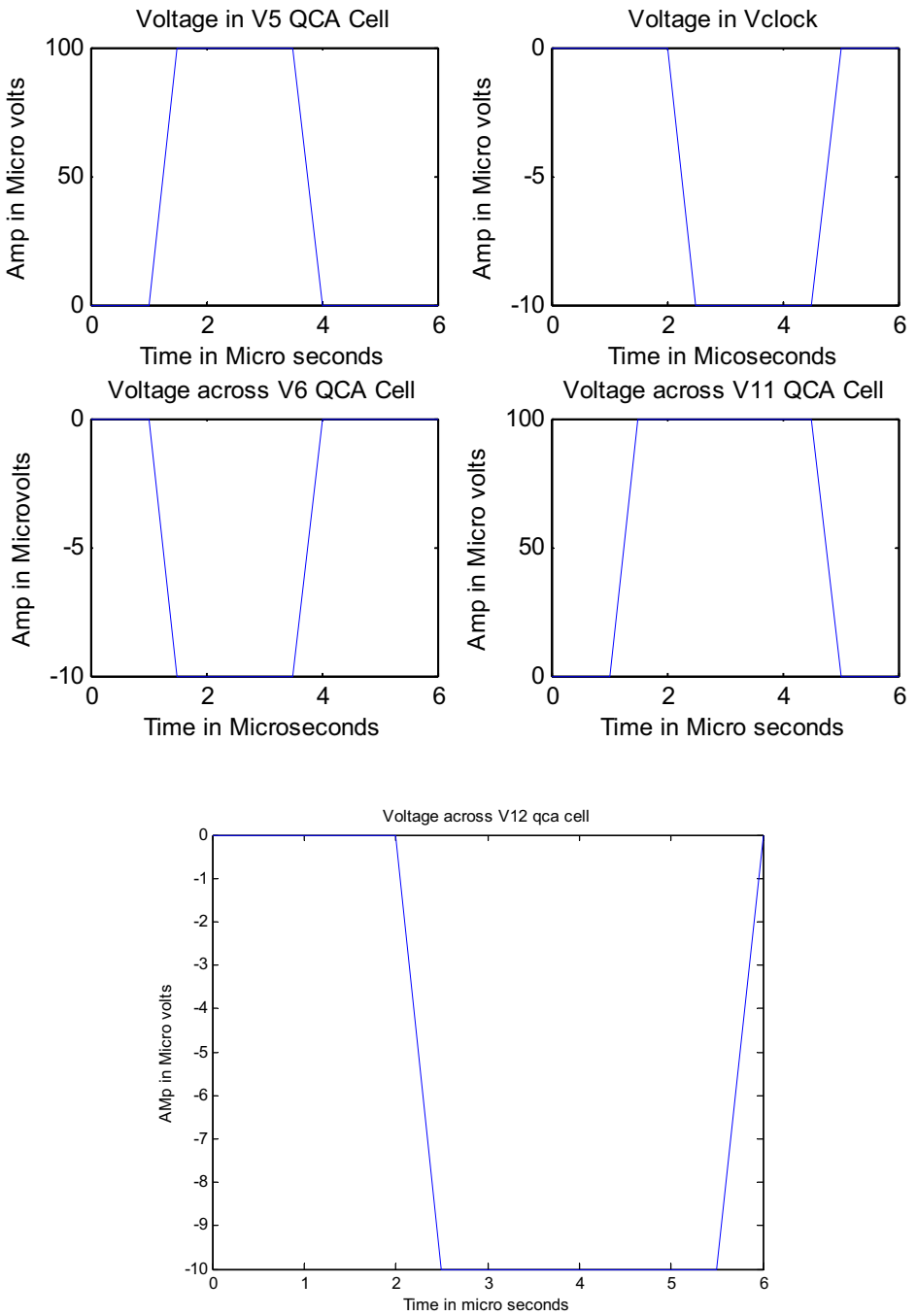

Figure 12 voltage in microvolts vs. time in microseconds with clock applied to Majority gate QCA circuit.

Figure 12 shows the sequence of input and clock applied to majority gate of QCA circuit. Initially input of 100 micro volts given to majority gate, when the clock applied externally to the cell is latched low then the input voltage is available to the middle cell at a time of 20 to 40 microseconds as in figure 12. The simulation is performed with Voltage clock of -10 microvolt and output V11 and V12 are obtained at 20 to 40 microseconds.

From 0 to 10 micro seconds, no switching occurs, From 10 to 20 microseconds again no switching due to no clocking, at 20 to 30 microseconds clock goes low and hence input signal raises to 100 micro volts, now the output node voltage V11 and V12 (across R1 and R2) raises to 100 microvolts and follows the majority of the input depending on voltage stored on all the capacitor around the middle cell. In switching condition capacitor charged to the input voltage and when clock becomes high the stored charge released, thereby signal passed to the next phase. The charging and discharging across capacitor continuous whenever clock changes, therefore the work done by the capacitor is calculated by first calculating the charge stored on the input capacitors. The charge can be calculated from Q-V plot by measuring the area enclosed in the chart. This plot gives the sequence of events happening there by direction of charge – voltage loops. Figure 13(a) and (b) shows the Q-V plot of a majority gate, at t1 say 10 micro sec input capacitor charged figure 13(a) shows response to input for weak signal of 50 micro volts and 13(b) shows for the signal of 100 micro volts, when the capacitor charged to 100 microvolt at which the clock signal is lowered to – 10 microvolt, the output capacitor follows the input cell, so the output signal follows the input signal till t2 to t3 (20 to 40 microseconds), when clock signal raised high, the output signal goes down as input signal moved from 40 to 50 microseconds. At t2 in figure 13(a) Q-V plot charge decreases to t3 due to discharge of output capacitor and finally the output signal reaches to the original condition from t4 to t0, thereby the output capacitor is ready for charging for the next clock cycle. The energy required for initiate switching action is done by clock signal; hence output follows the input signal. Figure 13(b) shows the anticlockwise direction of Q- V plot for signal of 100 microvolt. The area enclosed by the period gram in Q-V plot gives directly shows charge stored in output capacitor i.e. work done by the input cell on center cell in the switching event. Figure 13 a and b shows the work done to transfer information from input cell to center of cell and work done by the center cell to the neighbouring cell. The power gain of the majority gate is the ratio of the area calculated in figure 13a to the area calculated in figure 13 b which is nearly 2. We have verified our calculation with J.Timler and CS Lent (2002) which gives similar results. The results obtained from this analysis can be used to find power gain of practical QCA circuits.

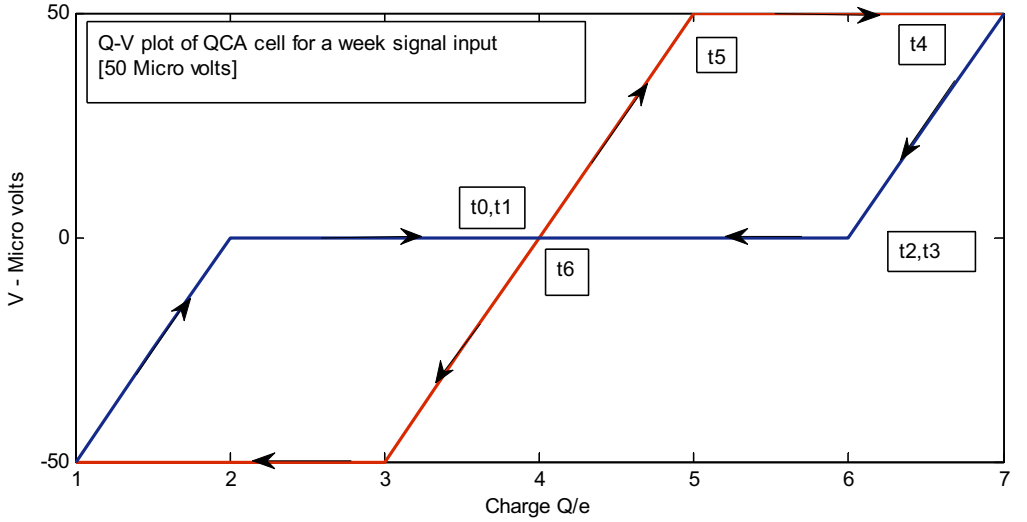

Figure 13 (a) Theoretical Q-V plot of QCA cell for a week signal input [50 Micro volts]

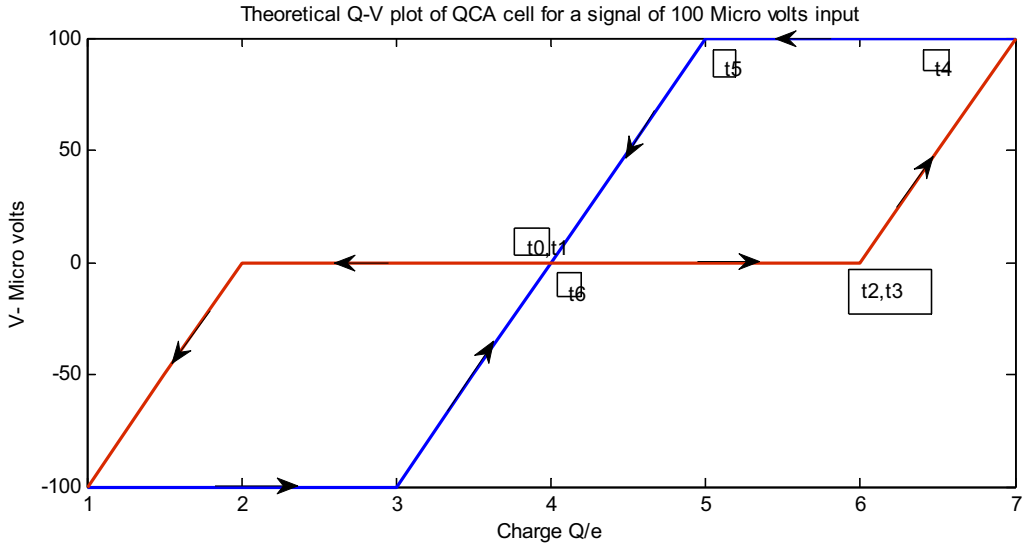

Figure 13 (b) Theoretical Q-V plot of QCA cell for a signal of 100 Micro volts input

4 Conclusion

QCA Simulation with the calculation of equivalent energy of any QCA circuit can be analyzed and power dissipation of a circuit can be found using the net energy flow equations. Energy equations are used to find the upper bound power model of a QCA circuit which can be used to find the maximum power dissipation of a cell in a QCA circuit. It was found that the maximum power dissipation is due to unlike inputs in a switching event than same inputs to QCA circuit. A upper bound power model is used as a tool to calculate power dissipation of Majority gate, Nand gate, and Multiplexer and Serial OR array QCA circuit. Also here theoretical power gain of a Modelled majority QCA gate circuit in a serial OR array can be calculated. Q-V plots of simple QCA Circuit are analysed for calculation of power gain of a majority gate. This theoretical analysis is used to study power dissipation and gain in a QCA technology.

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